Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **INPUT (2 pads)**
2. **OUTPUT (2 pads)**
3. **GND**

**.090”**

**1**

**2**

**0**

**E**

**1**

**2**

**3**

**2**

**1**

**MASK REF**

**NOTE: Chip back must be connected to INPUT.**

**.069”**

**Top Material: Al**

**Backside Material: Au or Si**

**Bond Pad Size: .004” X .004” min.**

**Backside Potential: Input**

**Mask Ref: 120E**

**APPROVED BY: DK DIE SIZE .069” X .090” DATE: 7/11/22**

**MFG: NATIONAL THICKNESS .010” P/N: LM120KG-12 MD8**

**DG 10.1.2**

#### Rev B, 7/19/02